IN THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (New) Method for testing a testable electronic device (200) having a first plurality of test arrangements (220), a second plurality of test arrangements (240), a first shift register (210, 250) having a plurality of cells (212; 214; 216; 252; 254; 256) and a second shift register (230, 270) having a plurality of cells (232; 234; 236; 272; 274; 276), each cell of the first shift register (210, 250) being coupled between an external pin and one of the test arrangements (222, 224, 226) from the first plurality of test arrangements (220) and each cell of the second shift register (230, 270) being coupled between an external pin and one of the test arrangements (242, 244, 246) from the second plurality of test arrangements (240), the method comprising the steps of:

serially communicating first test data (102, 106) between a first shift register (110, 150, 210, 250, 410, 450) and a first test data channel (202, 206, 402, 406), and at least partially simultaneous therewith, serially communicating second test data (104, 108) between a second shift register (130, 170, 230, 270, 430, 470) and a second test data channel (204, 208, 404, 408); and

parallelly communicating the first test data (102, 106) between the first plurality of test arrangements and the first shift register (110, 150, 210, 250, 410, 450), and at least partially simultaneous therewith, parallelly communicating the second test data (104, 108) between the second plurality of test arrangements and the second shift register (130, 170, 230, 270, 430, 470).

17. (New) A method as claimed in claim 16, comprising the further steps of copying the first test data (102, 106) from the first shift register (110, 410) into a first buffer register (120, 420) and copying the second test data (104, 108) from the second shift register (130, 430) into a second buffer register (140, 440).

18. (New) A method as claimed in claim 16, wherein:

the step of serially communicating the first test data (102) is directed from the first test data channel (202, 402) to the first shift register (110, 210, 410);

the step of serially communicating the second test data (104) is directed from the second test data channel (204, 404) to the second shift register (130, 230, 430);

the step of parallelly communicating the first test data (102) is directed from the first shift register (110, 210, 410) to the first plurality of test arrangements; and

the step of parallelly communicating the second test data (104) is directed from the second shift register (130, 230, 430) to the second plurality of test arrangements.

19. (New) A method as claimed in claim 18, comprising the further steps of:

parallelly receiving first test result data (106) from the first plurality of test arrangements in a third shift register (150, 250, 450), and at least partially simultaneous therewith, parallelly receiving second test result data (108) from the second plurality of test arrangements in a fourth shift register (170, 270, 470); and

serially submitting the first test result data (106) from the third shift register (150, 250, 450) to a third test data channel (206, 406), and at least partially simultaneous therewith, serially submitting the second test result data (108) from the fourth shift register (170, 270, 470) to a fourth test data channel (208, 408).

20. (New) A testable electronic device (200), comprising:

a first plurality of test arrangements (220) and a second plurality of test arrangements (240);

a first external pin (202, 206) and a second external pin (204, 208);

a first shift register (210, 250) register having a plurality of cells, each cell being coupled between an external pin and one test arrangement of the first plurality of test arrangements (220), a first cell being coupled to the first external pin (202, 206) for serially communicating first test data with the first external pin (202, 206), and for parallelly communicating the first test data with the first plurality of test arrangements (220); and

a second shift register (230, 270) having a plurality of cells, each cell being coupled between an external pin and one test arrangement of the second plurality of test arrangements (240), a first cell being coupled to the second external pin (202, 206) for serially communicating second test data with the second external pin (204, 208) at least

partially simultaneous with the serial communication of the first test data, and for parallelly communicating the second test data with the second plurality of test arrangements (240) at least partially simultaneous with the parallel communication of the first test data.

21. (New) A testable electronic device (200) as claimed in claim 20, wherein the first shift register (210) is arranged to communicate the first test data from the first external pin (202) to the first plurality of test arrangements (220), and the second shift register (230) is arranged to communicate the second test data from the second external pin (204) to the second plurality of test arrangements (240), and wherein the electronic device (200) further comprises:

a third external pin (206) and a fourth external pin (208);

a third shift register (250) having a plurality of cells, each cell being coupled between an external pin and one test arrangement of the first plurality of test arrangements (220), a first cell being coupled to the third external pin (206) for serially submitting first test result data to the third external pin (206), and for parallelly receiving the first test result data from the first plurality of test arrangements (220); and

a fourth shift register (270) having a plurality of cells, each cell being coupled between an external pin and one test arrangement of the second plurality of test arrangements (240), a first cell being coupled to the fourth external pin (208) for serially submitting second test result data to the fourth external pin (208) at least partially simultaneous with the serial submission of the first test result data, and for parallelly receiving the second test result data from the second plurality of test arrangements (240) at least partially simultaneous with the parallel reception of the first test result data.